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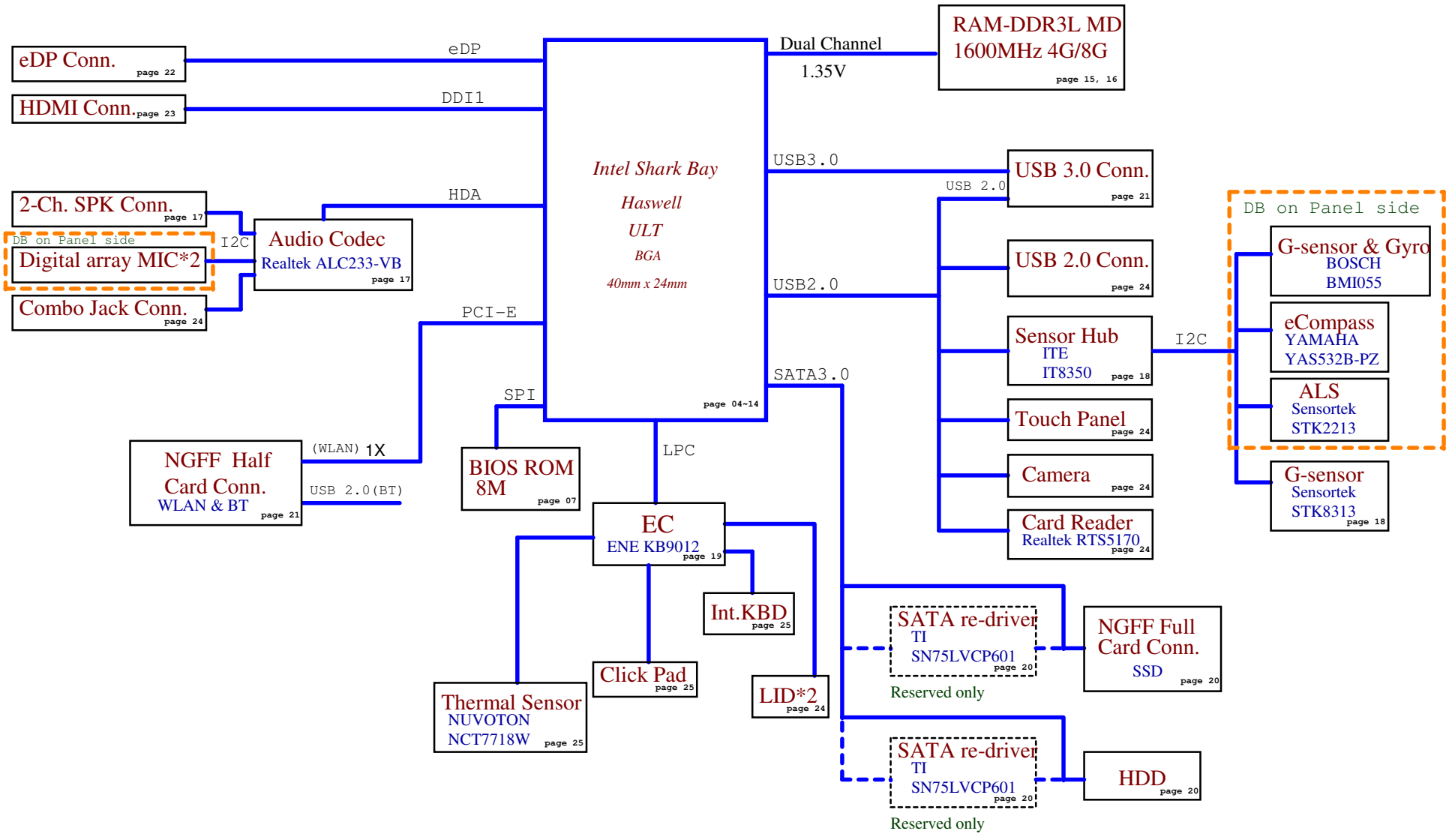
Model Name : ZIVY0  
File Name : LA-A921PR03  
BOM P/N:4319xxxxxx -- ZIVY0

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ZIVY0 M/B Schematics Document  
Intel SharyBay ULT Processor

2013-12-01  
REV : 1 . 0

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## Voltage Rails

power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
State				
S0	○	○	○	○
S3	○	○	○	×
S5 S4/AC	○	○	×	×
S5 S4/ Battery only	×	×	×	×
S5 S4/AC & Battery don't exist	×	×	×	×

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

## BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
Unpop	@
CPU OPTION	CPU1@ ~ CPU5@
DRAM Option	H4G@ E4G@ S4G@ M4G@ S8G@ E8G@ H8G@ H8G@
KB9012	9012@
KB9022	9022@
No Re-driver	NR@
TI Re-driver	TI@
PARADE Re-driver	8520C@
Segate HDD	HDDSG@
WD HDD	HDDWD@
EMI PART	EMI@
ESD PART	ESD@
SSD-SATA	SSDSATA@

## EC SM Bus1 address

Device	Address
Smart Battery Charger Home Key Button	01100000

## EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W SharkBay ULT SML1	1001100x

## CPU SM Bus address

Device	Address
Touch Pad	

## CPU SML0 Bus address

Device	Address
--------	---------

## USB 2.0 Port Table

USB 2.0	Port	2 External USB Port
	0	USB 2.0 Port (I/O Board)
	1	USB 3.0/2.0 Port (MB)
	2	
	3	Card Reader
	4	Touch Screen (reserve)
	5	Camera
	6	Mini Card (WLAN/BT)
	7	Sensor Fusion

## USB 3.0 Port Table

Port	
1	
2	USB 3.0 Port (MB)
3	
4	

## PCIe Port Table

Port	Lane	
1		
2		
3		
4		WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

## SATA Port Table

Port	
3	NGFF SSD(SATA)
2	
1	
0	HDD

## SMBUS Control Table

	HOST	Changer	BATT	KB9022	CPU	HomeKey	Touch Pad	Thermal sensor NCT7718W
EC_SMB_CK1	KB9022 +3VLP	+3VLP	+3VLP	×	×	+3VLP	×	×
EC_SMB_DA1	KB9022 +3VS	×	×	×	+3VS	×	×	+3VS
EC_SMB_DA2	CPU +3VALW	×	×	×	×	+3VS	×	×
SMBCLK	CPU +3VALW	×	×	×	×	×	×	×
SMBDATA	CPU +3VALW	×	×	×	×	×	×	×
SML0CLK	CPU +3VS	×	×	×	×	×	×	+3VS
SML0DATA	CPU +3VS	×	×	×	×	×	×	+3VS
SML1CLK	CPU +3VS	×	×	×	×	×	×	+3VS
SML1DATA	CPU +3VS	×	×	×	×	×	×	+3VS

## CPU part

U1 CPU1@ I7-4500U 1.8G C0 SA00006SLA0	U1 CPU2@ I3-4010U 1.7G C0 SA00006SX80	U1 CPU3@ I5-4200U 1.6G C0 SA00006SMC0	U1 CPU4@ I3-4100U 1.8G C0 SA00006SU30	U1 CPU5@ I3-4005U 1.7G D0 SA000072C50
---	---	---	---	---

## PCB part

ZZZ0 PCB 138 LA-A921P REV0 M/B 3 DA800020000
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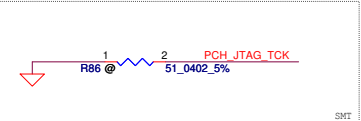
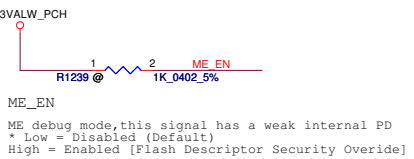
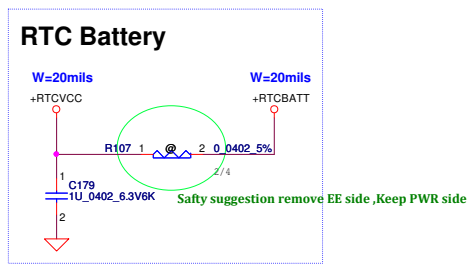
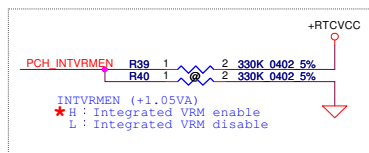
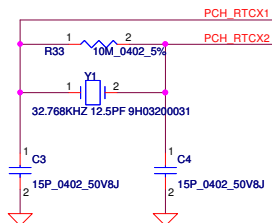
## DRAM

ZZZ3 H4G@ HYNIX X765263BL02	ZZZ4 E4G@ ELPIDA X765263BL03	ZZZ7 S4G@ SAMSUNG X765263BL01	ZZZ8 M4G@ MICRON X765263BL04	ZZZ9 S8G@ SAMSUNG X765263BL05	ZZZ10 E8G@ ELPIDA X765263BL07	ZZZ5 M8G@ MICRON X765263BL06	ZZZ6 H8G@ HYNIX X765263BL06
H5TC4G63AFR-PBA SA000005AV20	EDJ4216EFBG-GN-F SA000005BT40	K4B401646Q-HYK0 SA000005JC40	MT41K256M16HA-125:E SA000005WD10	K4B8G1646Q-HYK0 SA000005WD10	EDJ8416E6MB-GN-F SA000006AU00	MT41K512M16TNA-125E SA000006AV00	H5TC8G63AMR-PBA SA000006W200

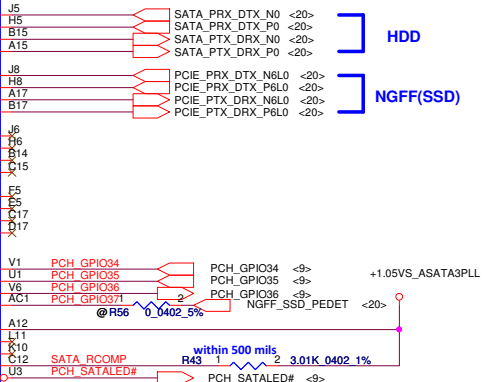
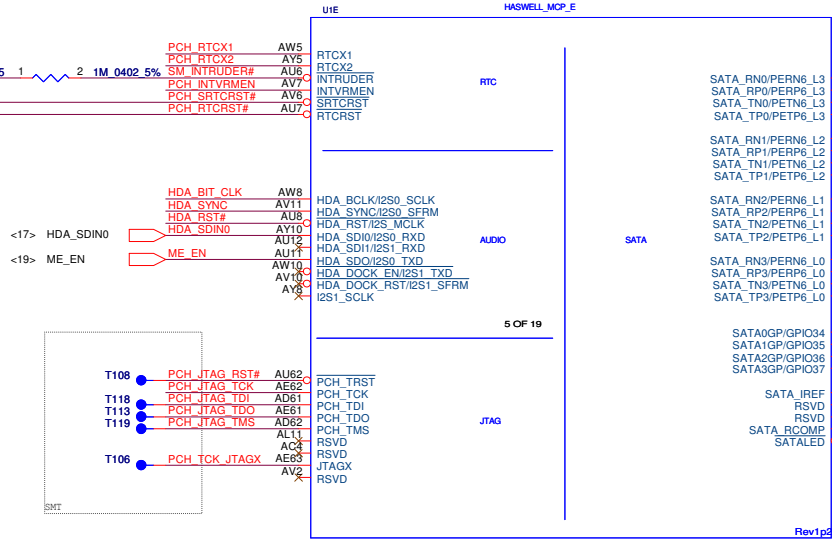
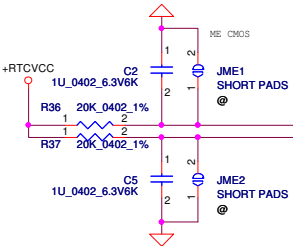
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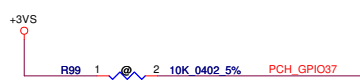
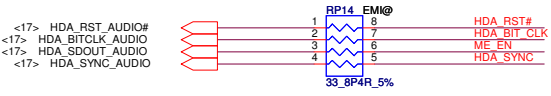




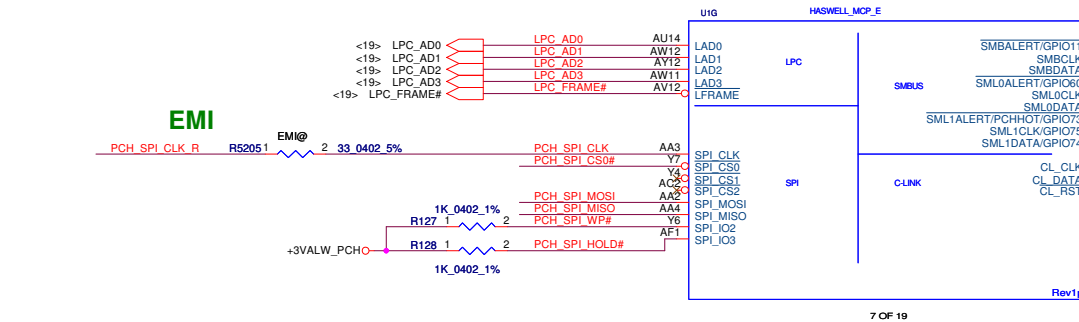
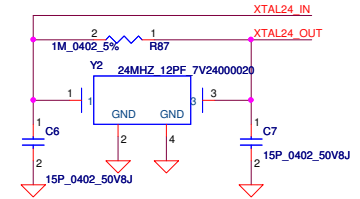
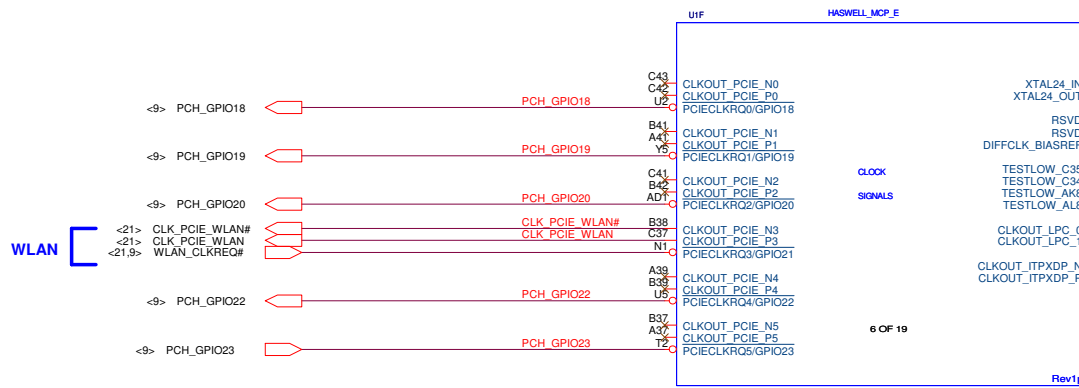
JME2 Short PAD placement to Bottom side.



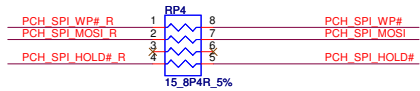
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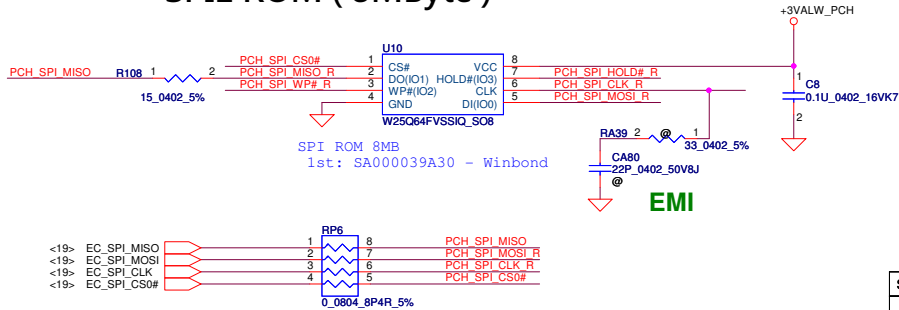
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Issued Date				2013/07/24				Title			
Deciphered Date				2015/07/24				HWSW MCP(3/11) RTC,SATA,XDP			
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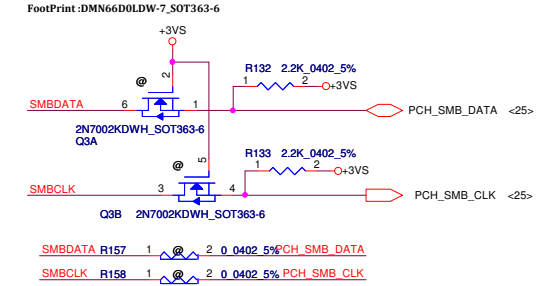
CHKLIST1.0  
2 SPI Device = 33 ohm  
1 SPI Device = 15 ohm



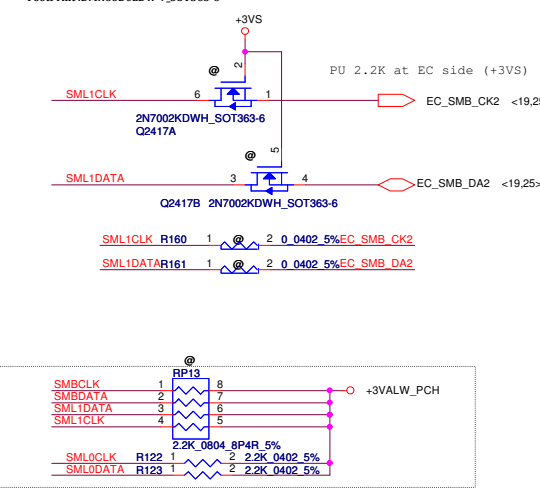
## SPI1 ROM ( 8MByte )



## SMBus :TP



## SML1 Bus :EC/Thermal Sensor



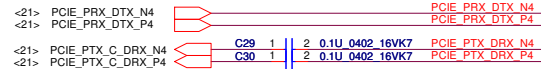
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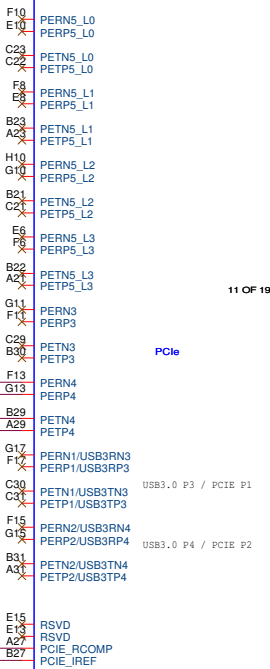




WLAN



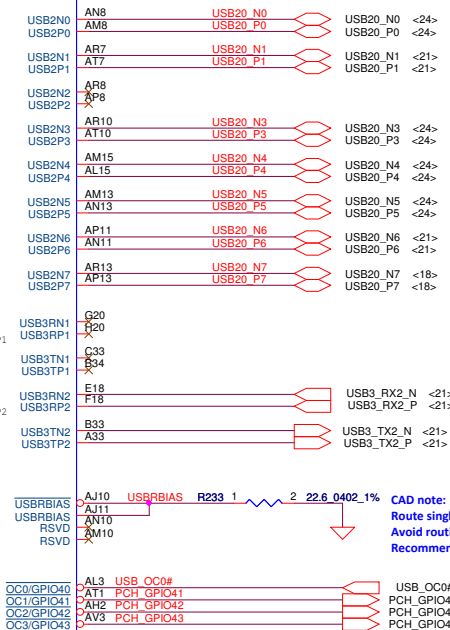
U1K HASWELL\_MCP\_E



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PCie

USB



USB2 IO (Sub Board)

USB2/3 IO (Main Board)

Card Reader

Touch Screen

Camera

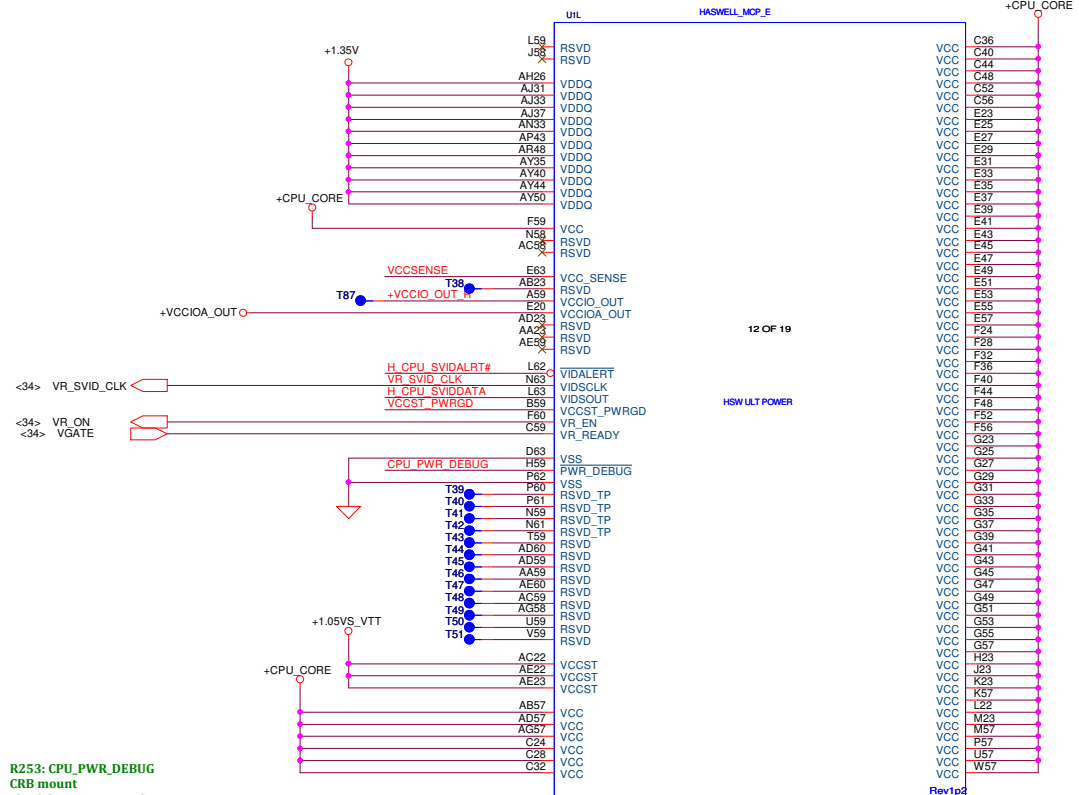
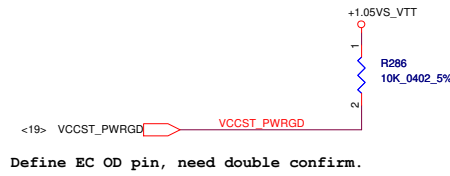
Mini Card(WLAN+BT)

Sensor

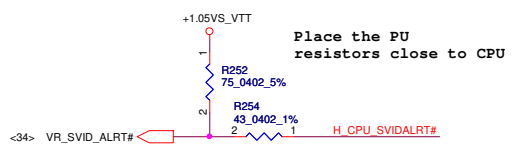
USB2/3 (Main Board)

CAD note:  
Route single-end 50-ohms and max 450-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils

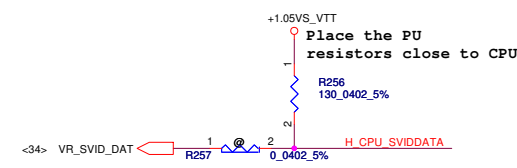
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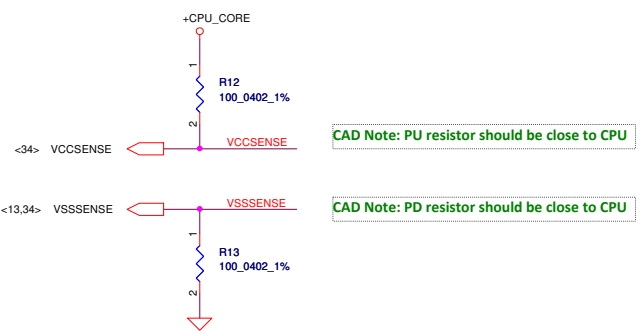
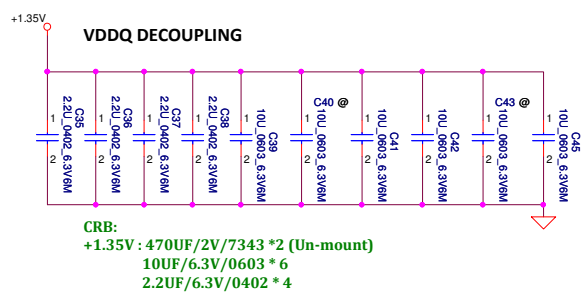
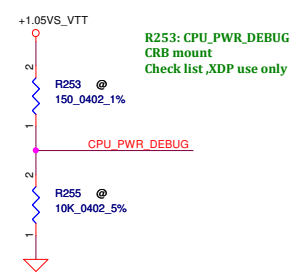
### SVID ALERT



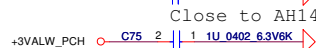
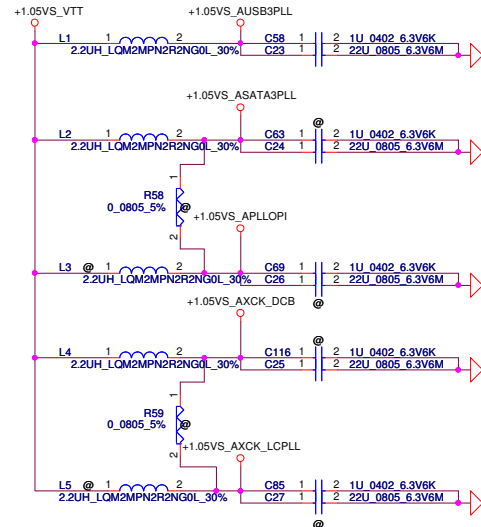
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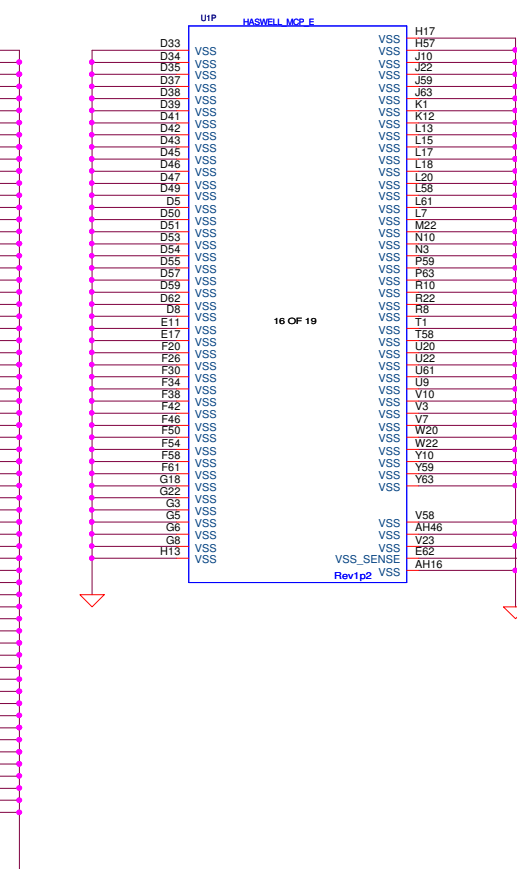
R256:  
CRB r0.7 changed from 130 Ohms to 110 Ohms



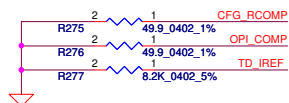
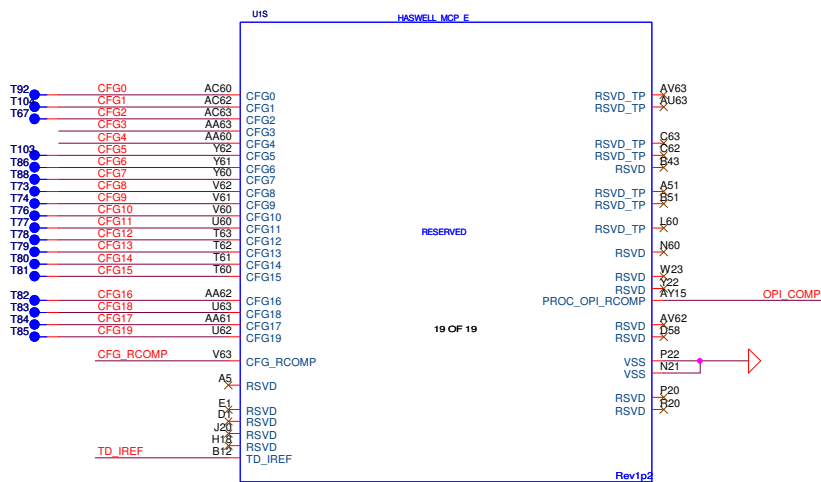
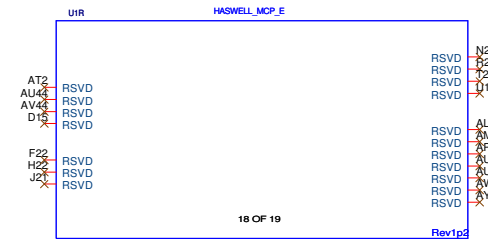
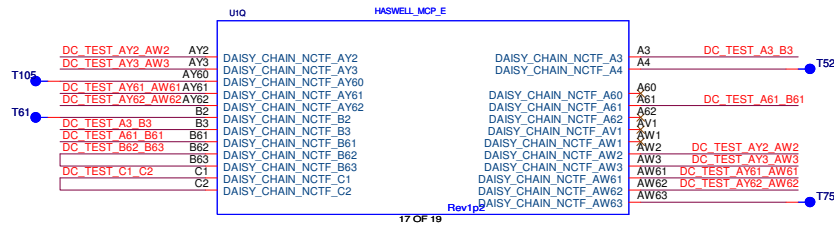
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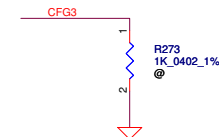
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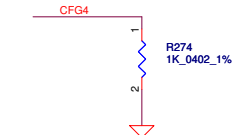
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## CFG Straps for Processor



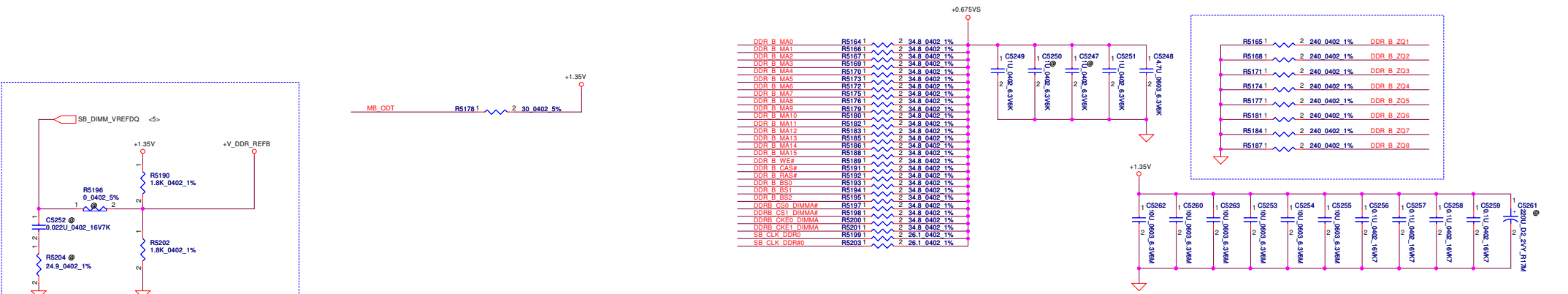
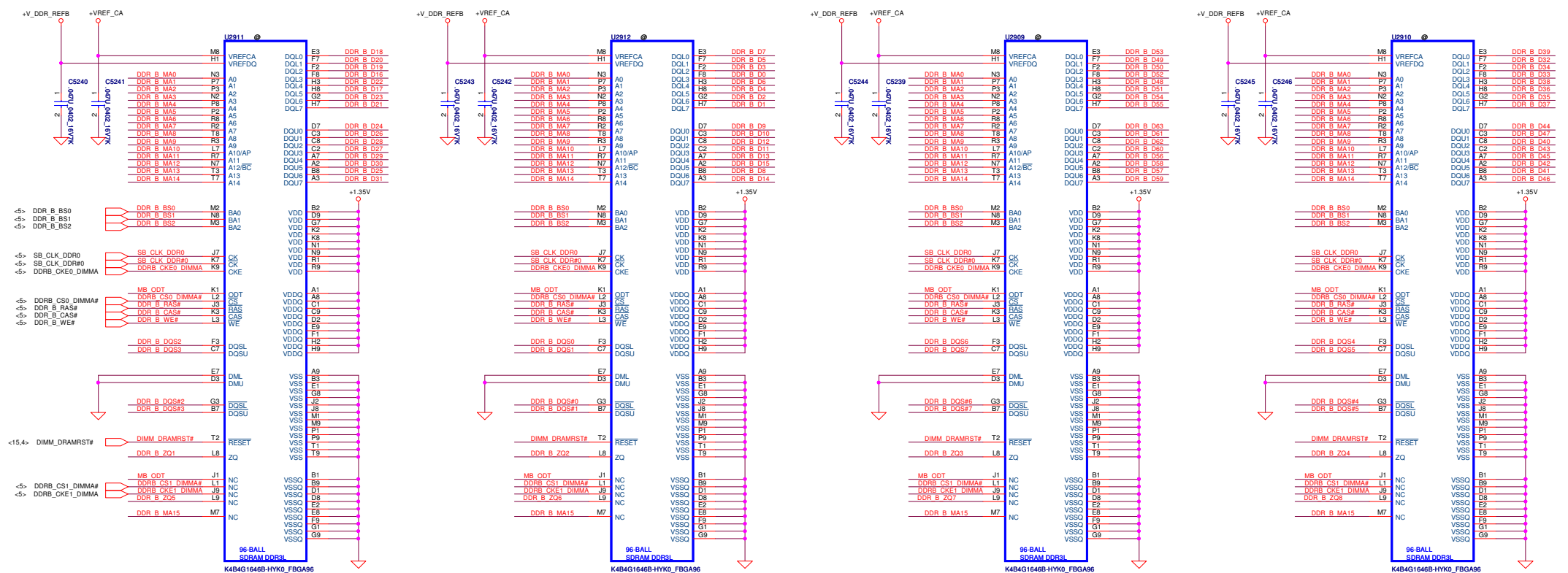
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

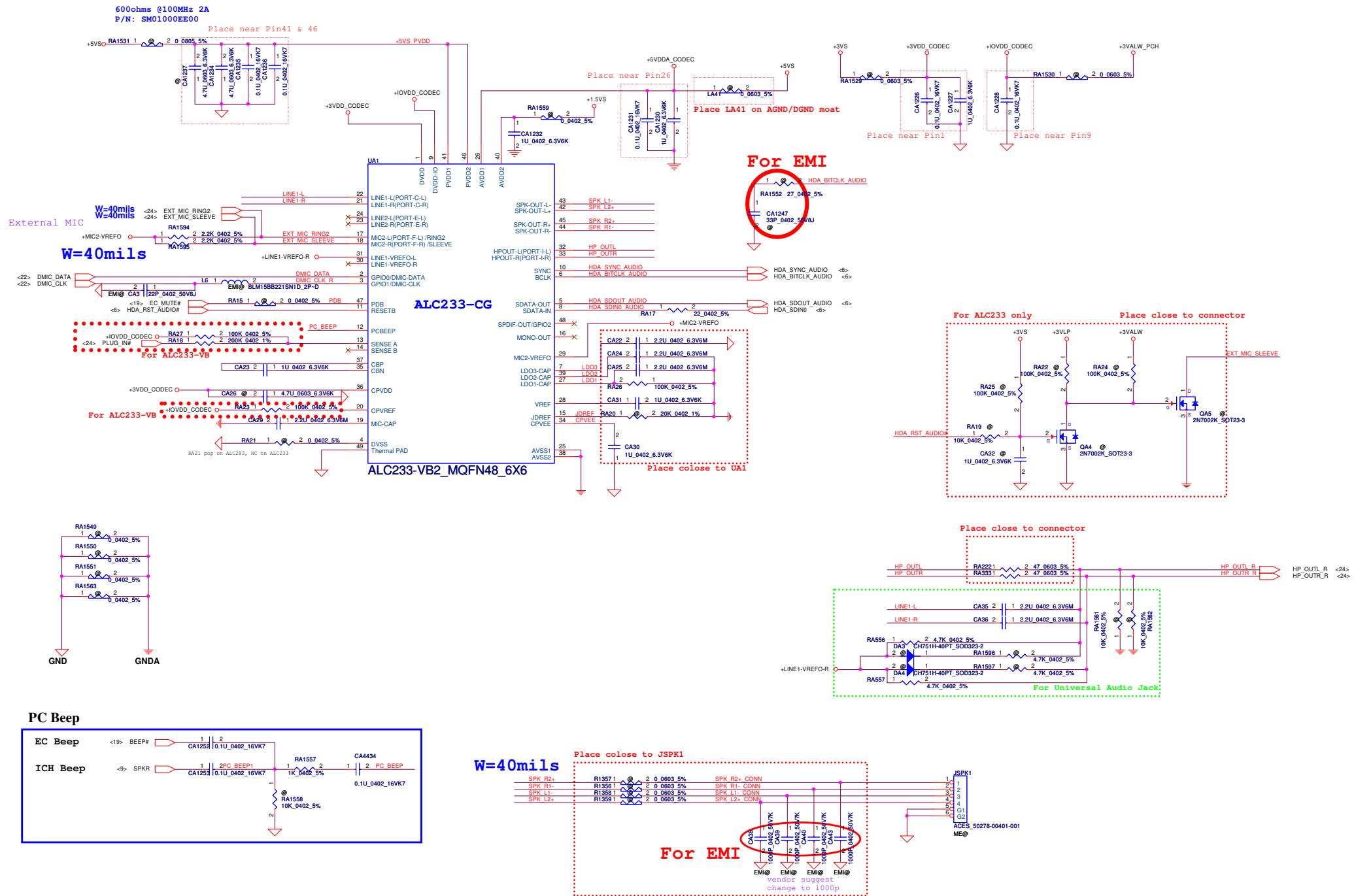
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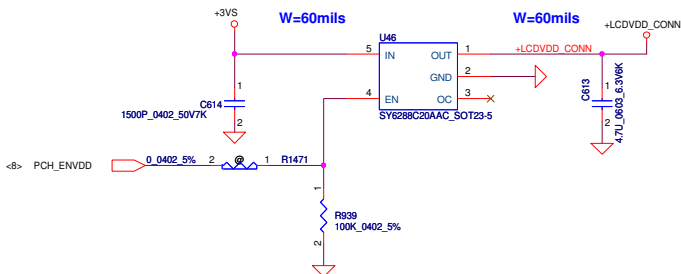




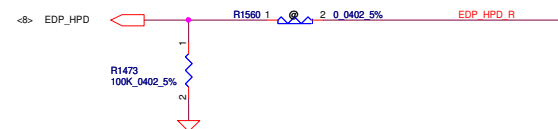
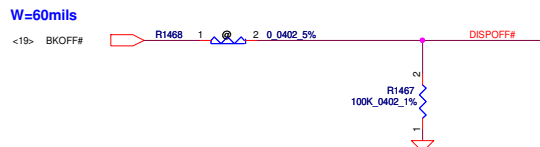
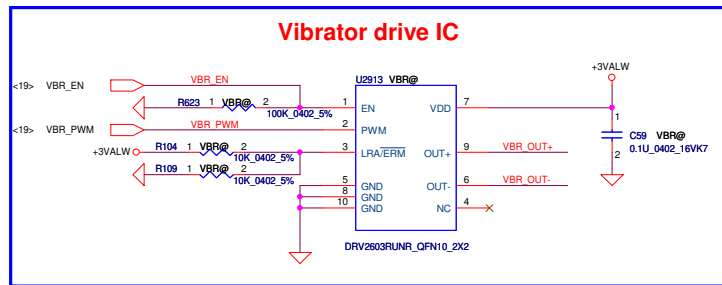




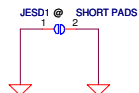
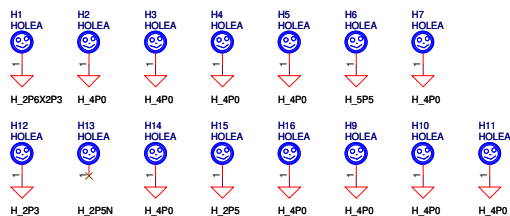
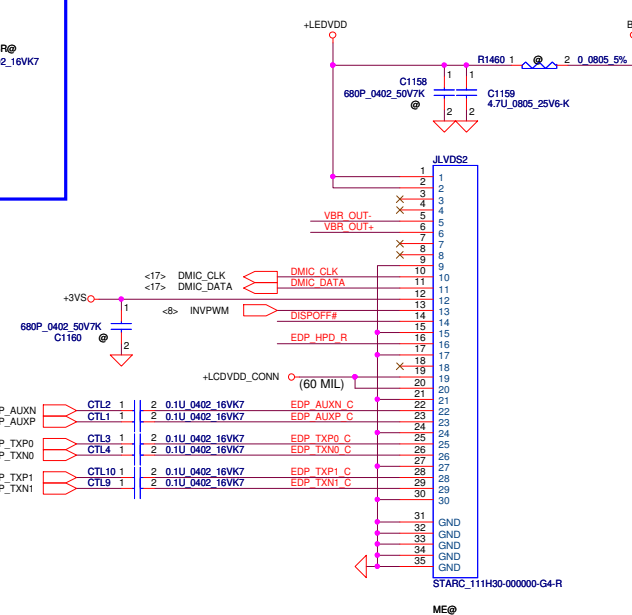
## LCD POWER CIRCUIT



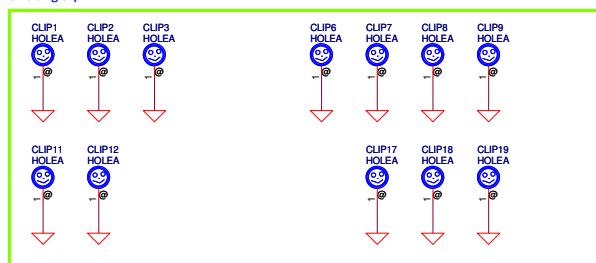
RTD2132R Internal load switch for +LCD\_VCC



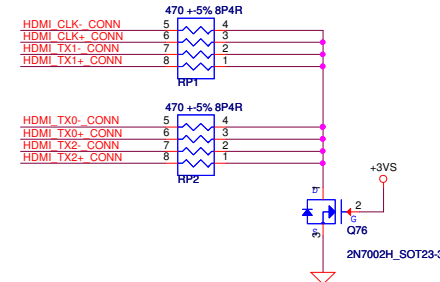
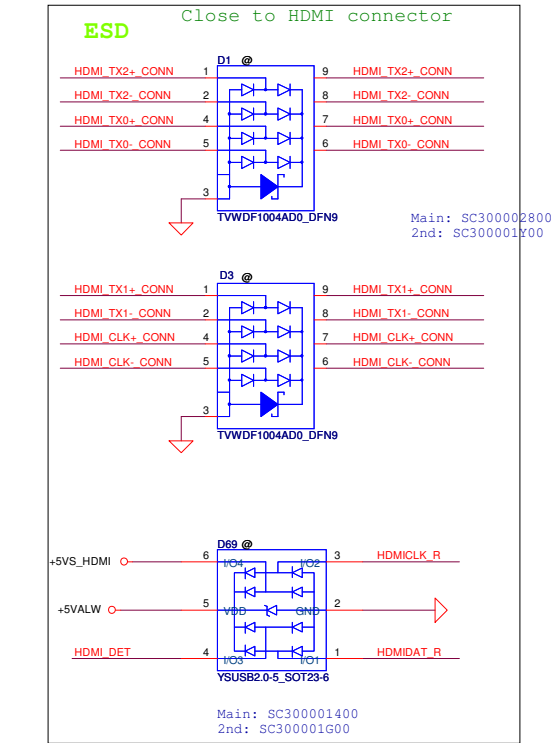
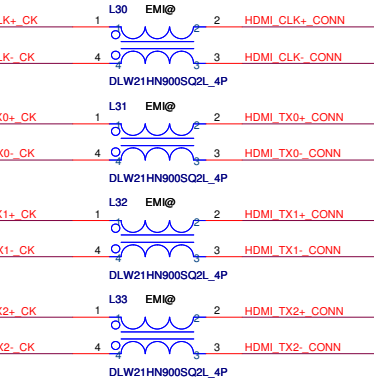
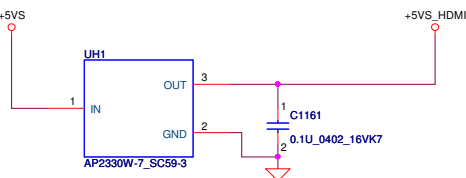
## eDP PANEL BD. Conn.



### Shielding Clip

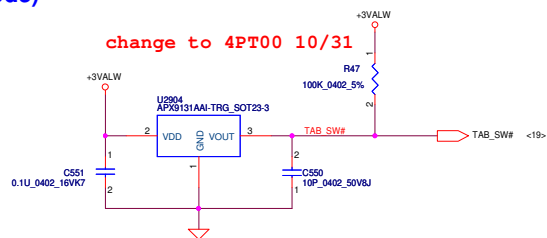


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Title		Compal Electronics, Inc.	
Size		eDP /DMIC/ HOLE	
Document Number		LA-A921PR01	
Date		Tuesday, December 17, 2013	
Sheet		22 of 38	

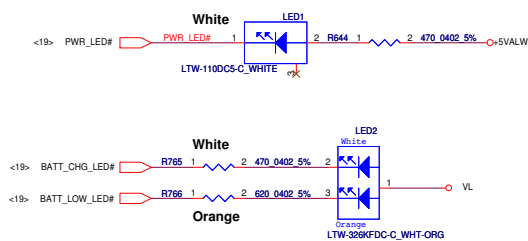


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				Customer	1.0
				Date: Tuesday, December 17, 2013         Sheet 23 of 36	

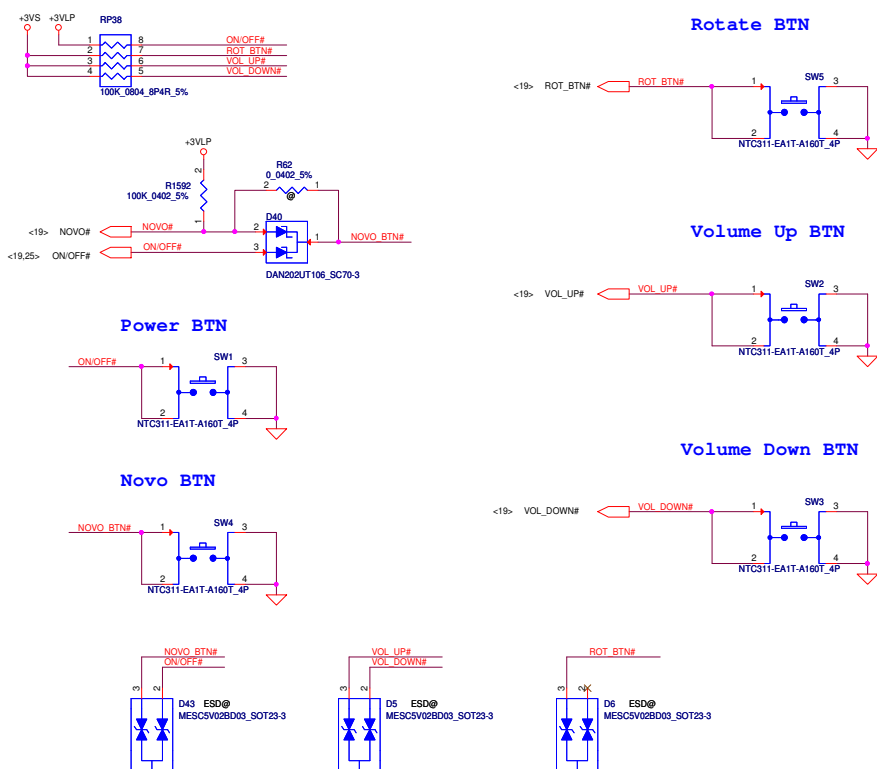
# Lid SW(Tablet Mode)



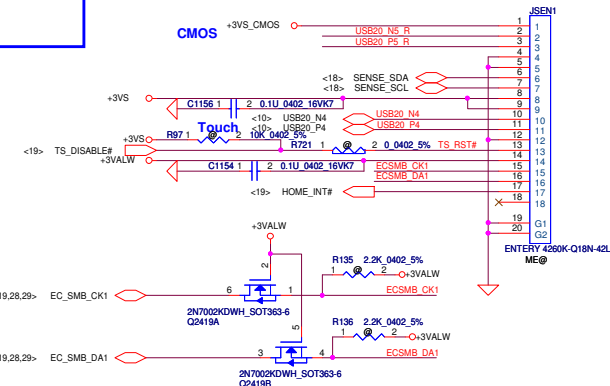
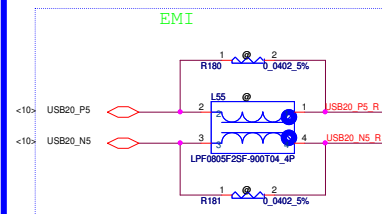
# LED



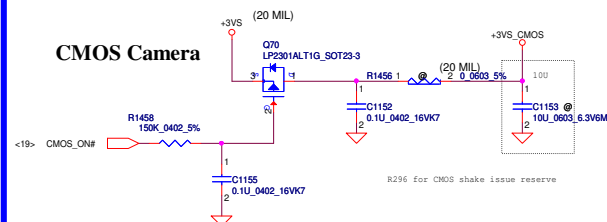
# BUTTON



# Touch & CMOS Conn

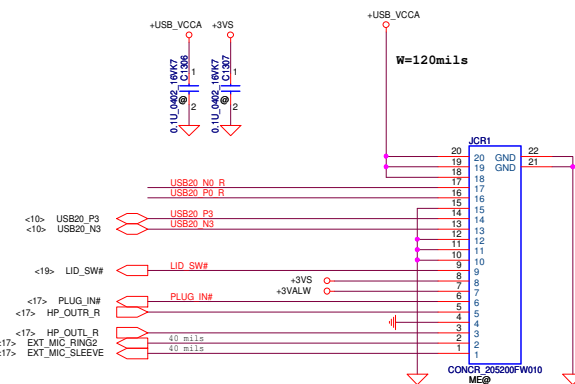
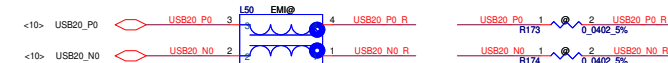


# CMOS Camera



# I/O Board

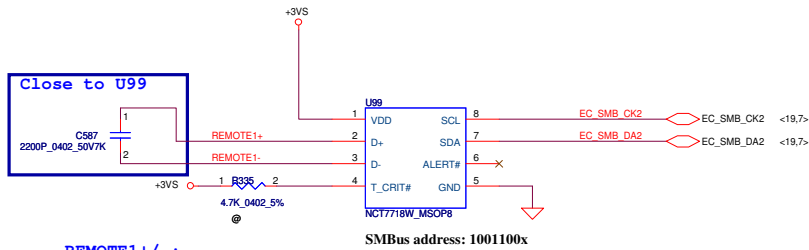
## EMI



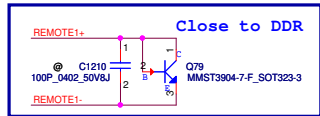
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Issued Date		Deciphered Date		Document Number	
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Rev		1.0		Rev	



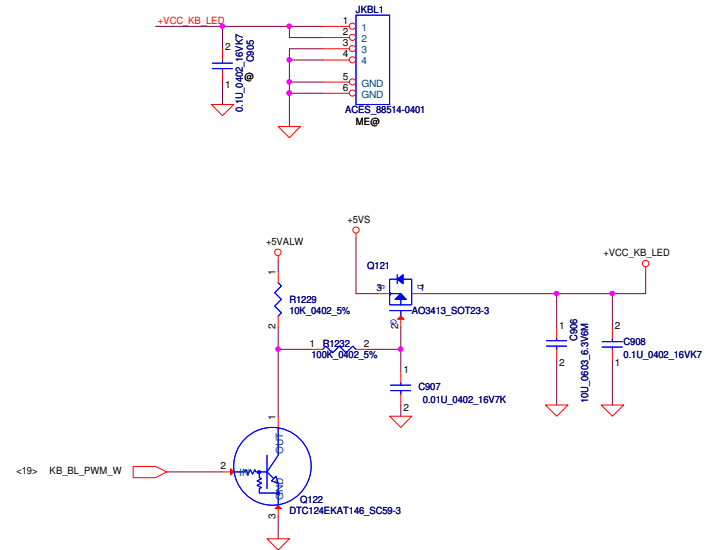
## Thermal Sensor



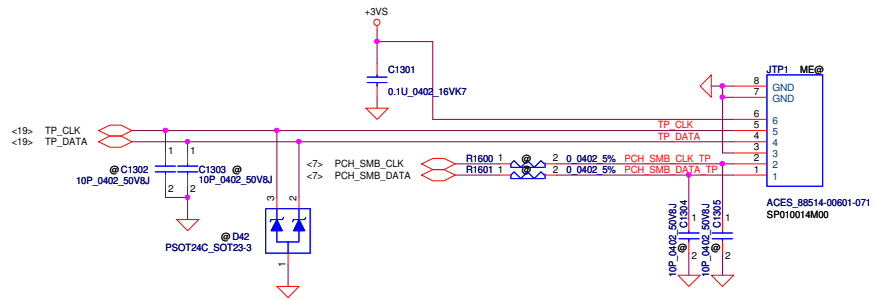
```
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"
```



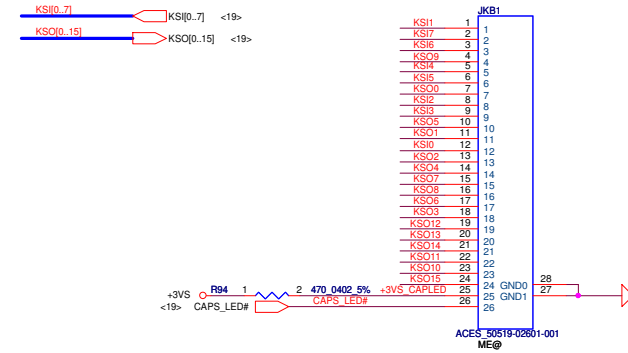
## Keyboard Backlight



### Click Pad

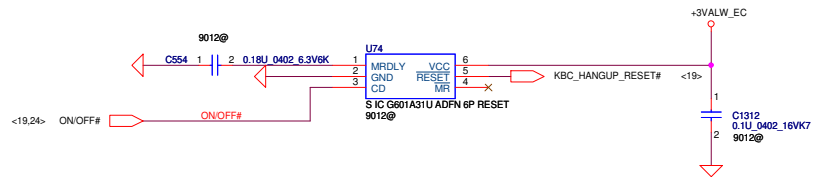


## Keyboard



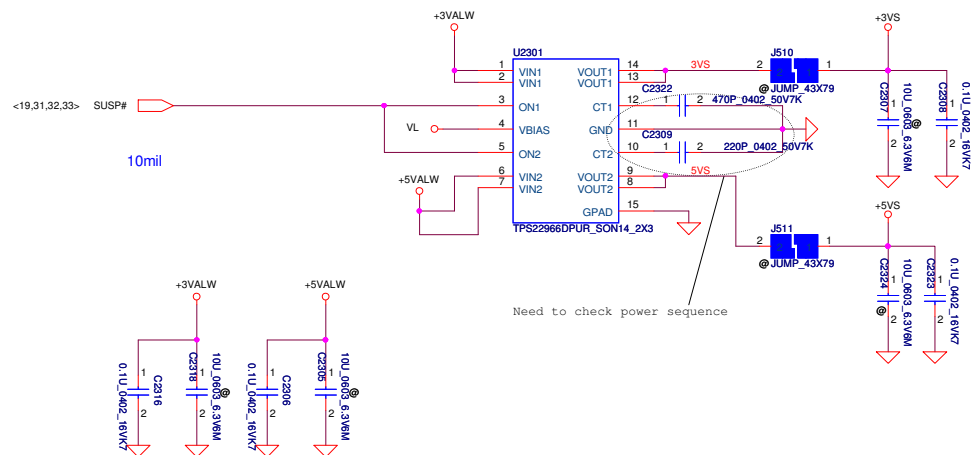
## EC Reset IC

## EC RESEST function

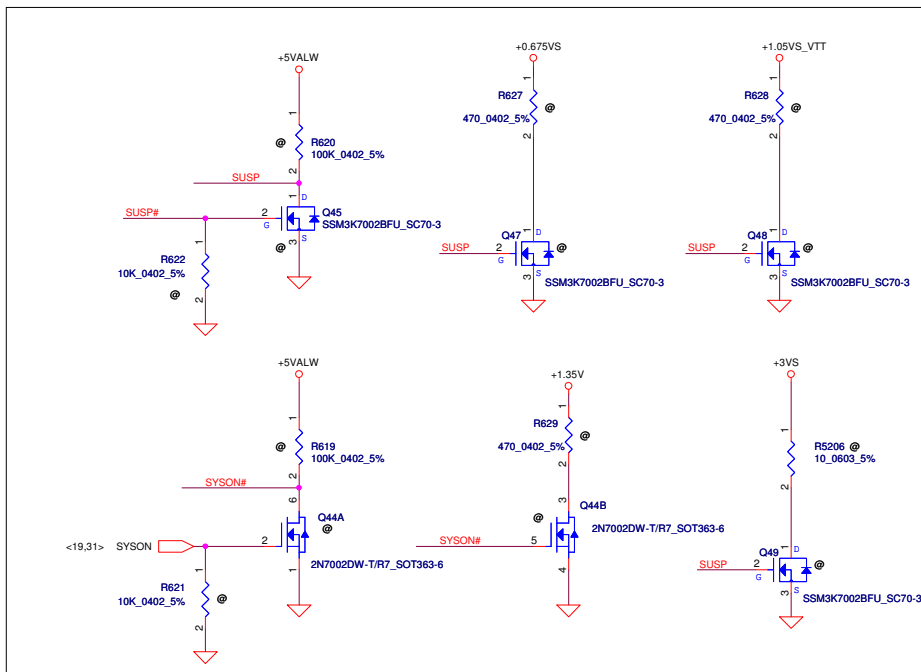


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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title	<b>KB/TP/Thermal Sensor</b>	
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				Date:	Tuesday, December 17, 2013	Sheet

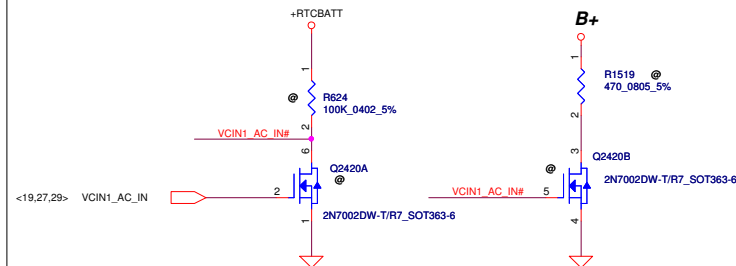
+5VALW TO +5VS  
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)  
+5VALW TO +5VALW(PCH AUX Power)



## B+ discharger



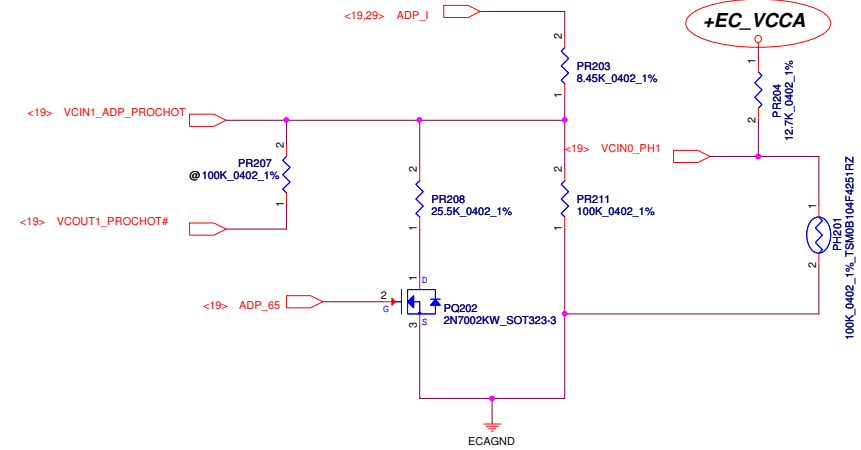
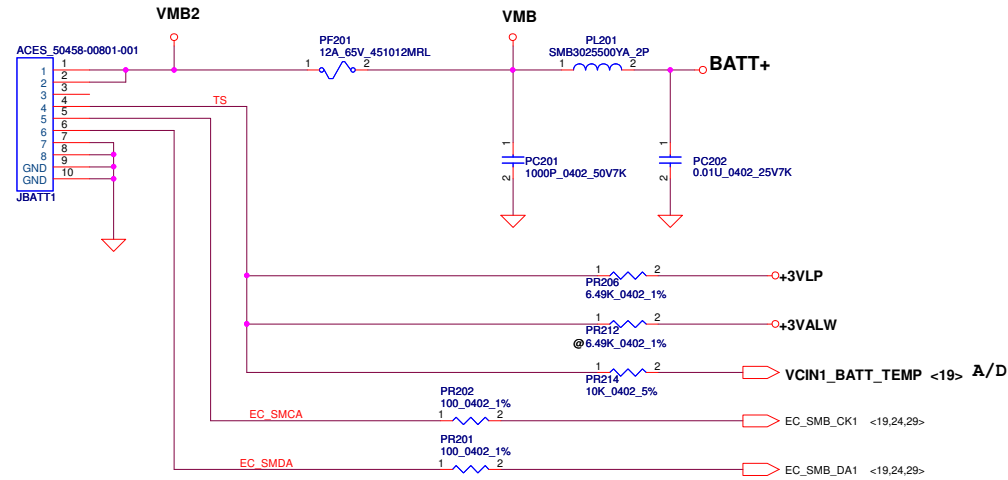
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Issued Date				2013/07/24				Deciphered Date			
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PH201 under CPU botten side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C

65W(UMA): 85W active W recovery

20120314  
Change to +EC\_VCCA from +3VLP



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# Module model information

BQ24715\_V2.mdd

65W adapter support NVDC  
BQ24715 support 2, 3 cell  
BQ24717 for 4 cell

H/MOS  
Rds(on) = 24m ohm(typ), 30m ohm(Max.)  
power loss= 0.9944W  
L/MOS  
Rds(on) = 9.9m ohm(typ), 13m ohm(Max.)  
power loss= 0.3396W  
Pd of Choke = 0.9892W

## Vin Detector

	Min.	Typ	Max.
L-->H	17.578V	17.755V	17.933V
H-->L	17.023V	17.349V	17.674V

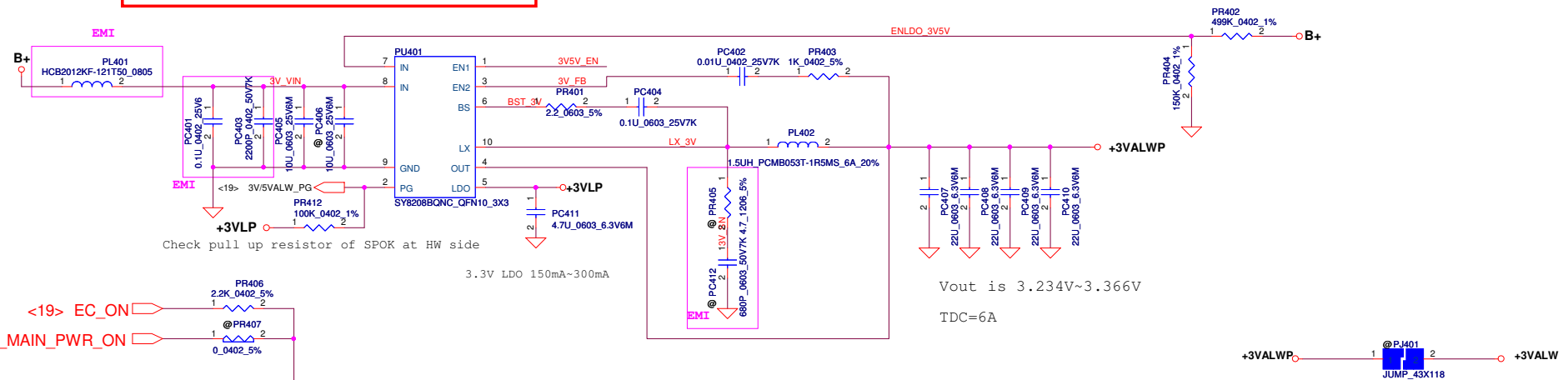
placement near EC

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Date: Tuesday, December 17, 2013				Rev 1.0

# Module model information

SY8208B\_V2.mdd

EN1 and EN2 don't floating

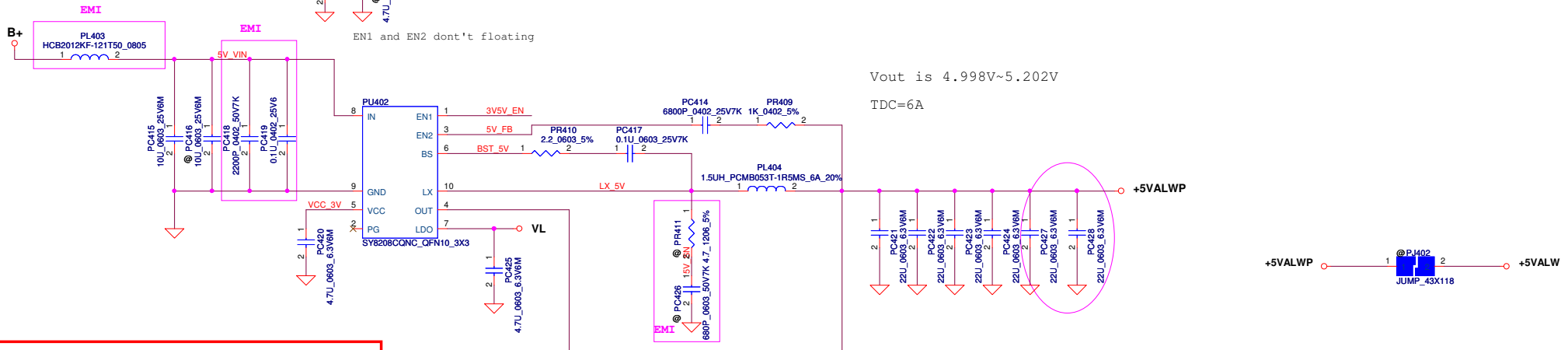


<19> EC\_ON

<19> VCOUT0\_MAIN\_PWR\_ON

EC VDD0 is +3VL, PC13 UNPOP  
EC VDD0 is +3VALW, PC13 POP

EN1 and EN2 don't floating



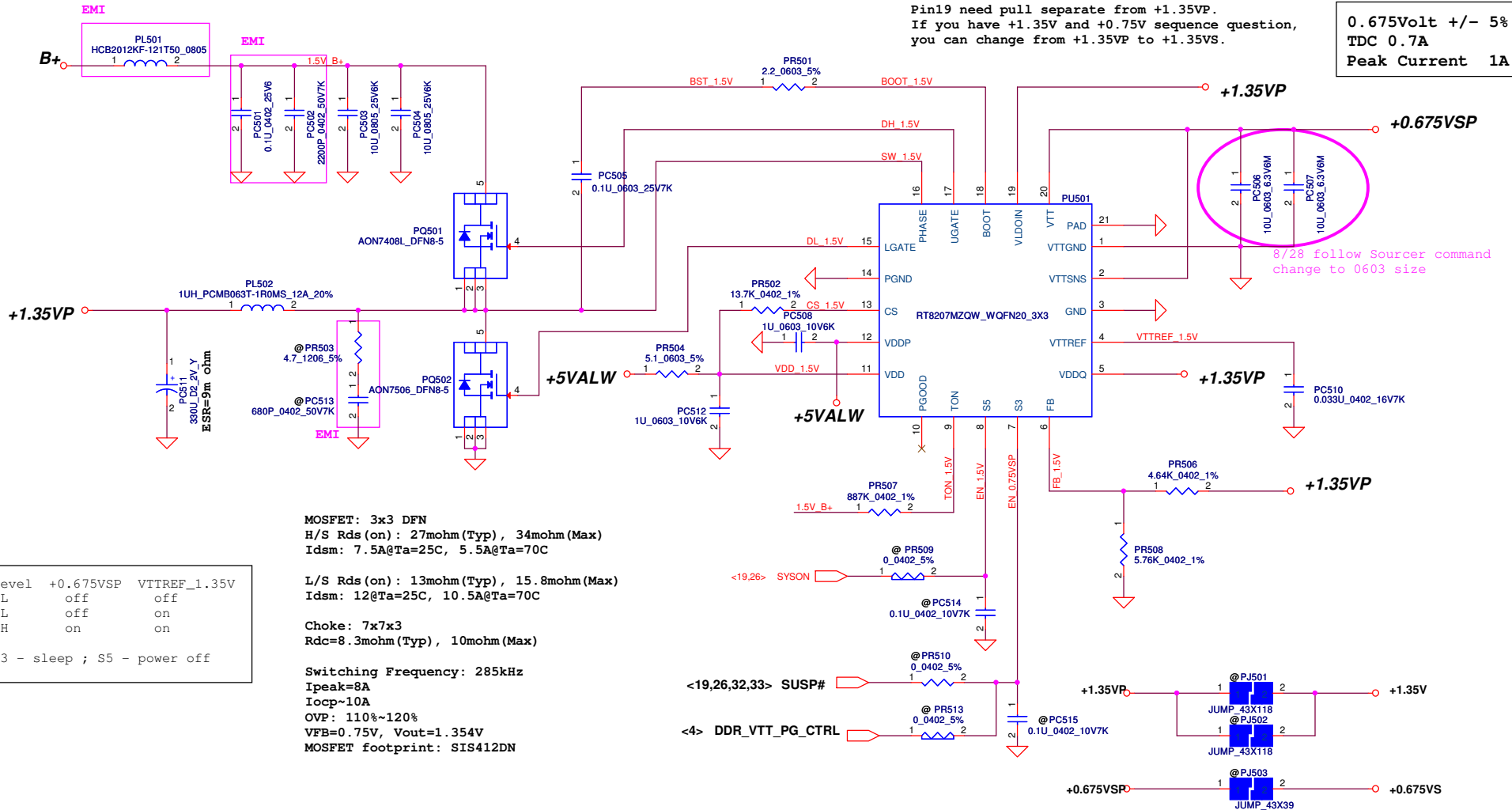
# Module model information

SY8208C\_V2.mdd

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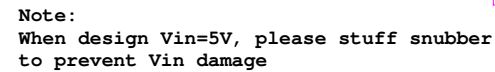
# Module model information

RT8207M\_V1.mdd For Single layer  
RT8207M\_V2.mdd For Dual layer



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						Size Custom	Document Number			Rev 1.0	
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SY8003\_V1.mdd



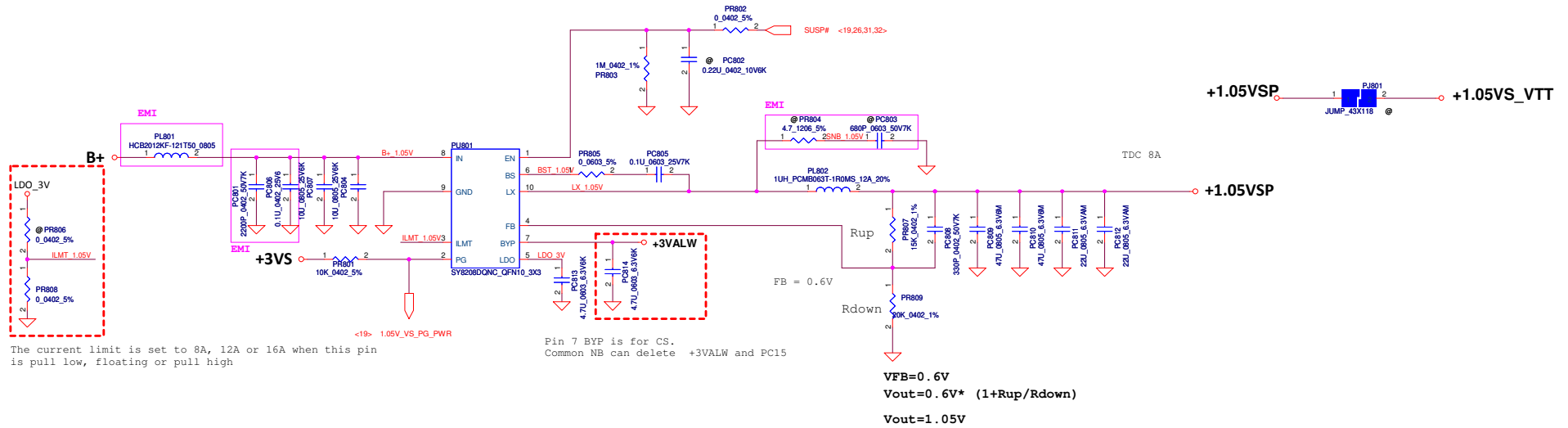
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$
$$V_{out} = 1.5V$$



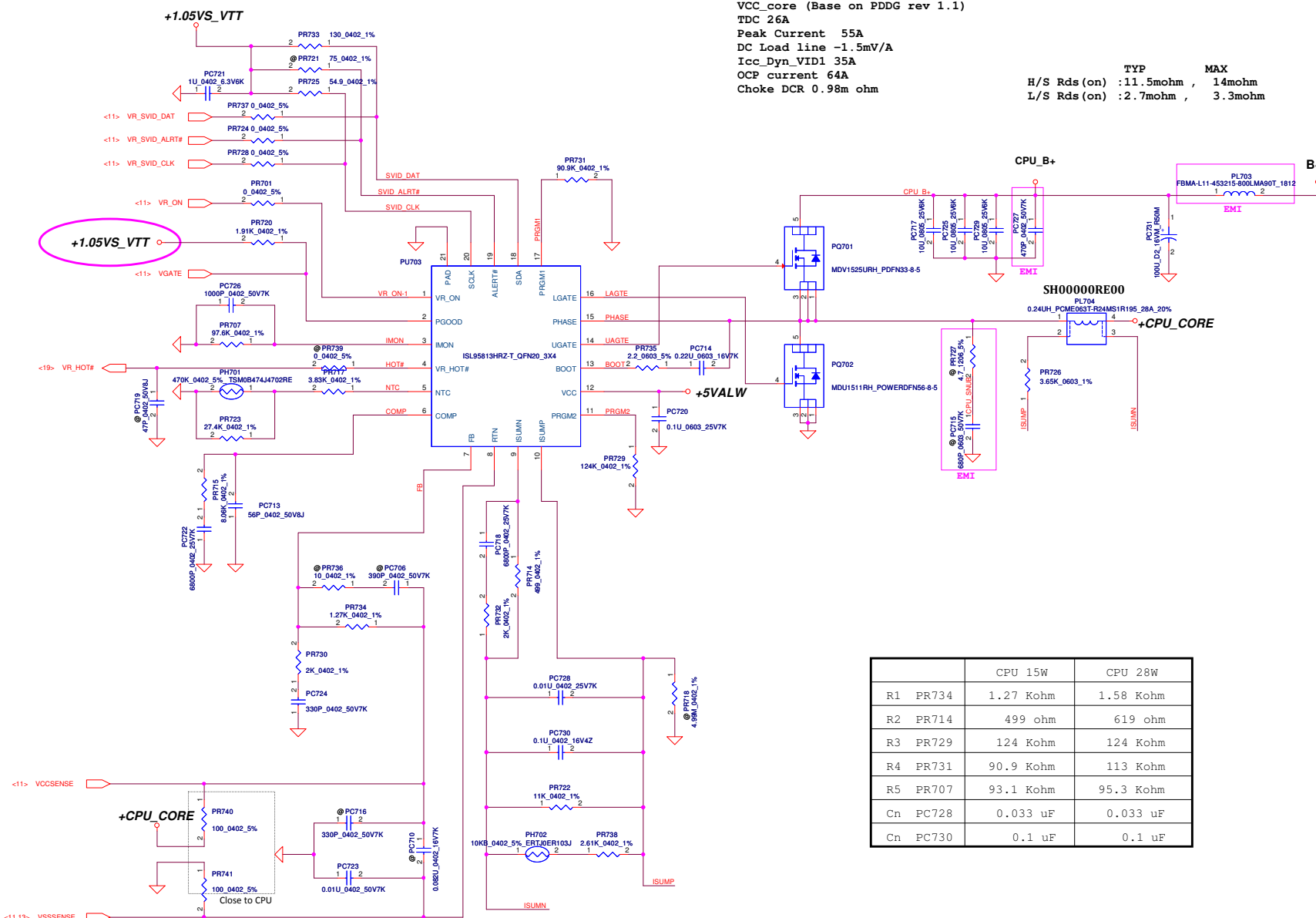
# Module model information

SY8208D\_V1.mdd

EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



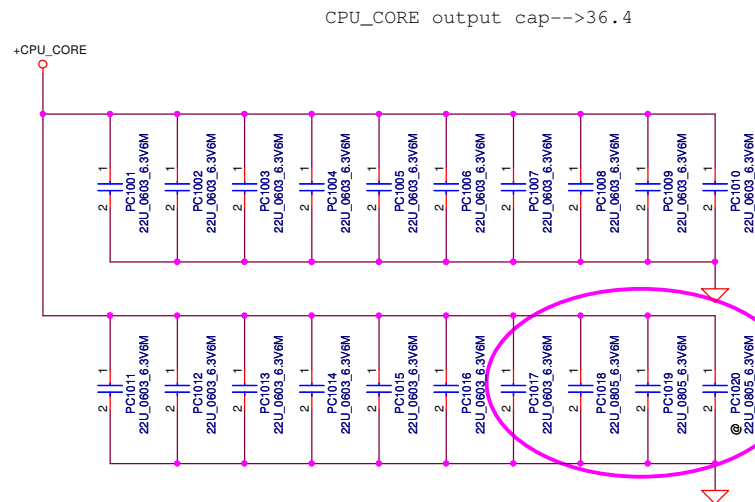
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VCC\_core (Base on PDDG rev 1.1)  
TDC 26A  
Peak Current 55A  
DC Load line -1.5mV/A  
Icc\_Dyn\_VID1 35A  
OCP current 64A  
Choke DCR 0.98m ohm

TYP MAX  
H/S Rds (on) :11.5mohm , 14mohm  
L/S Rds (on) :2.7mohm , 3.3mohm

	CPU 15W	CPU 28W
R1 PR734	1.27 Kohm	1.58 Kohm
R2 PR714	499 ohm	619 ohm
R3 PR729	124 Kohm	124 Kohm
R4 PR731	90.9 Kohm	113 Kohm
R5 PR707	93.1 Kohm	95.3 Kohm
Cn PC728	0.033 uF	0.033 uF
Cn PC730	0.1 uF	0.1 uF



30 X 22uF 0805  
2012/10/23  
check the output cap Qty!!!  
2012/10/24  
23 pcs 22uF and reserve 7 pcs  
2013/01/14  
22uF\*15; reserve 22uF\*5

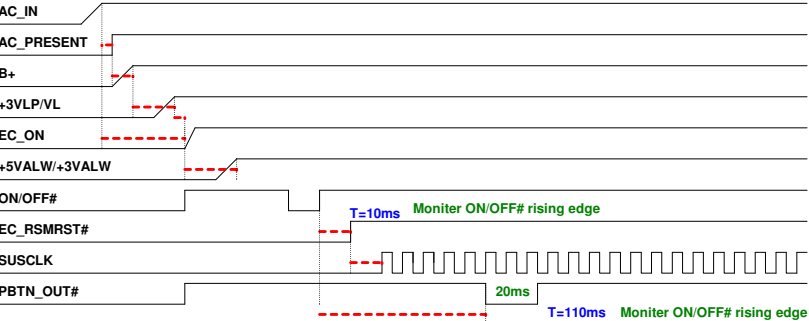
2013/09/6 22U\_0603x17 + 22U\_0805x2

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Item	Reason for change	PG#	Modify List	Phase
1	For ME design change	21,23	JHDMI1,JUSB1 change connector type	EVT
2	For ME design change	24	SW1,SW2,SW3,SW4,SW5 change type	EVT
3	For ME design change	24,25	JCR1,JKB1 change connector type	EVT
4	For EC pin common design	19	EC pin 25,27,38,86,123 control pin change	EVT
5	Follow EC power plane for EC_Reset	25	Change U74 power plan	EVT
6	For DVT phase MB ID	19	R1564 change from 43K to 27K	EVT
7	For BDW HDMI request	23	RP1,RP2 change value from 680ohm to 470ohm	EVT
8	For Audio vender recommend	17	1. Un-mount RA19,RA22 2. Mount RA1551,RA1563 3. Add CA1,CA2	EVT
9	For EMI request	17	R55 change to Bead	EVT
10	For Compal component policy	9,21	U52,U4 change type	EVT
11	For touch vennder recommend	24	1. JSEN1 pin 13 add 10K pull high 2. JSEN1 pin 14 change to +3VALW	EVT
12	For SPEC change	6,20	Delete SSD PCIE interface component	EVT
13				
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[DC Mode]

